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Development and Evaluation of a GaAs MMIC Phase-Locked Loop Chip Set for Space Applications

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***Abstract*—GaAs monolithic microwave integrated circuit (MMIC) chips designed for a phase-locked loop frequency source to be used in space applications have been developed. The chip set includes a three-stage resistive feedback amplifier (RFA) with 13 dB gain in a 275 MHz to 5.85 GHz bandwidth, a 2.0 GHz voltage-controlled oscillator (VCO), a 2.8 GHz digital prescaler, and a VHF/UHF digital phase/frequency discriminator. Both analog and buffered-FET logic (BFL) digital circuits were fabricated on the same wafer. The MMIC process which was developed for this application comprises molecular beam epitaxial (MBE) deposition of the active layer, proton isolation, submicron gates, thin-film TaN resistor deposition, and silicon nitride passivation. The chip set was used successfully to implement a 2.0 GHz all-GaAs phase-locked loop (PLL).**

I. INTRODUCTION

MMIC's will have a major impact on communication satellite payloads of the future. One area of direct application is in fixed-frequency local oscillators (LO's) which are used for frequency mixing circuits throughout modern payloads. Conventional hybrid LO's are both bulky and heavy, making them highly unsuitable for phased array antenna applications.

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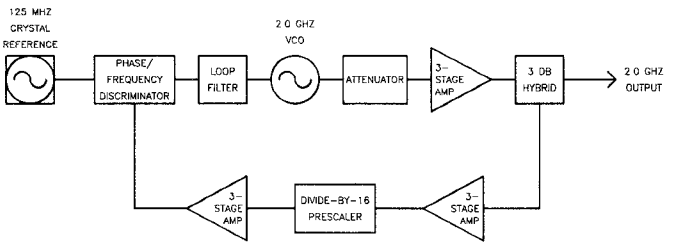


Fig. 1 GaAs MMIC phase-locked loop block diagram

Development of a generic GaAs PLL chip would greatly reduce the weight, size, and cost of an LO reference source while providing inherent radiation hardness. The stabilization of a microwave frequency source and the reduction of off-carrier noise density by means of a crystal oscillator and PLL have been described by Ohira *et al.* [1]. Additionally, MMIC chips suitable for use in PLL's have been reported [2]–[5]. In this paper, the implementation of MMIC's in a GaAs PLL integrated on a single breadboard is described. The basic analog and digital building blocks (the RFA, prescaler, VCO, and phase/frequency discriminator) have been fabricated monolithically on a single GaAs wafer and assembled into a MMIC PLL. The PLL design approach, processing technology, individual chip results, loop integration, and noise reduction will be discussed.

II. PHASE-LOCKED LOOP DESIGN

The primary goal of this project was to develop a 2.0 GHz MMIC PLL chip for use as an LO in satellite payloads. By designing a PLL with a wide capture range, a generic LO chip could be used in different satellite applications whereby the mere selection of a crystal reference would determine the LO frequency. Fig. 1 shows a block diagram of the MMIC/MIC phase-locked loop developed to this point. The PLL is a classical second-order design having passive *RC* loop filtering. The PLL has a 125 MHz crystal reference source that feeds the digital phase/frequency discriminator. A 2.0 GHz common-gate VCO provides the PLL microwave signal, while resistive-feedback amplifiers (RFA's) supply gain where needed in the loop. A prescaler scales the 2.0 GHz signal for feedback into the phase/frequency discriminator.

III. PROCESS DESCRIPTION

The process developed for the fabrication of the chips described in this paper comprises the following features:

- molecular beam epitaxial (MBE) deposition of the active layer,
- isolation of the active regions by proton-induced damage,
- thin-film tantalum nitride resistors,
- 0.75-μm-gate FET's,
- Schottky level-shifting diodes,
- metal–insulator–metal (MIM) capacitors with silicon nitride dielectric,
- air bridge second level interconnections (Fig. 2),
- silicon nitride passivation.

The MBE material, deposited sequentially on an undoped semi-insulating substrate, consists of a 0.4-μm-thick undoped

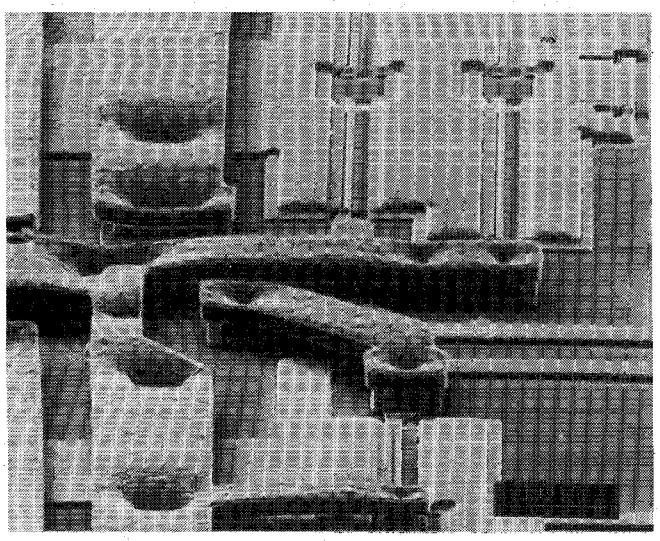


Fig. 2. SEM of second level air bridge metallization.

TABLE I
PCM TEST RESULTS
(MEAN ± STANDARD DEVIATION ACROSS THE WAFER)

Saturated drain current, I_{DSS}	161 ± 81 mA/mm
Transconductance, g_m	195 ± 29 mS/mm
Pinch-off voltage, V_p	0.96 ± 0.51 V
Gate metal resistance	84.7 ± 7.7 ohm/mm
Ohmic Contact resistance	0.065 ± 0.004 ohm.mm
Sheet resistance of MBE layer	110.3 ± 4.2 ohm/sq.
Active layer carrier concentration	$3.9\times10^{17} \pm 1.9\times10^{16}$ cm^{-3}
Active layer carrier mobility	2870 ± 153 cm^2/Vs
Tantalum nitride sheet resistance	49.3 ± 5.3 ohm/sq.
MIM capacitance/area	243 ± 3 pF/mm^2

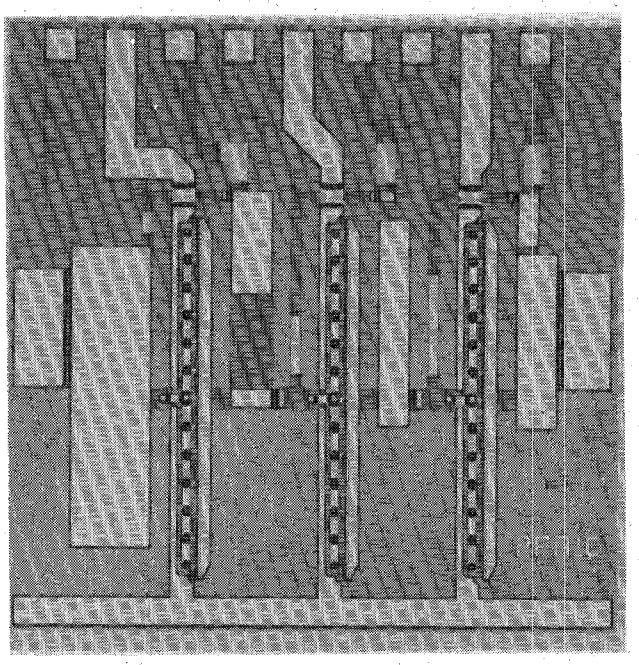
buffer layer; a 0.18-μm-thick, 4×10^{17} cm^{-3} silicon-doped active layer; and a 0.12-μm-thick 2×10^{18} cm^{-3} silicon-doped n+ layer to provide low-resistance ohmic contacts. The advantages of MBE include the possibility of selective deposition and integration of FET's and varactors requiring different doping profiles on the same chip. This is important for the final monolithic integration of the PLL. The completed wafer is lapped and polished to a final thickness of 400 μm and the back side is metallized with Ti–W/Au suitable for eutectic bonding of the chips into the final assembly.

The resistors, FET's, and diodes are passivated by a silicon nitride film deposited after the first-level metal interconnections have been completed. This silicon nitride film also provides the dielectric material for the MIM capacitors. The thin-film tantalum nitride resistors have a sheet resistance of 50 ohms/sq., a temperature coefficient of resistance in the range of -60 to $+30$ ppm, and are stable to at least 210°C at the maximum rated current density of 0.5 mA/μm.

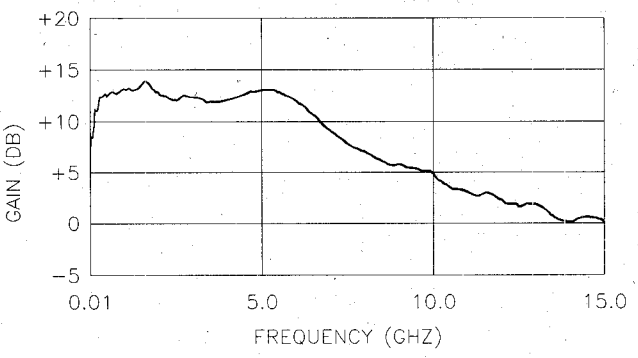
The process was characterized and monitored by means of a test pattern chip or process control monitor (PCM) similar to that described by Immorlica *et al.* [6]. The final PCM test results are presented in Table I. A 728 μm gate width FET was included on the PCM chip. This FET exhibited $f_t = 17$ GHz, $f_{max} = 40$ GHz, and a maximum available gain of 7.5 dB at 8 GHz.

IV. RESISTIVE-FEEDBACK AMPLIFIER CHIP

The monolithic RFA consists of three resistive feedback stages using 728 μm FET's in all three stages (Fig. 3(a)). The RFA typically displayed 13 dB gain with peak-to-peak ripple not exceeding 2 dB from 275 MHz to 5.85 GHz. Usable amplifier gain was shown from 10 MHz to 14.0 GHz (Fig. 3(b)).



(a)



(b)

Fig. 3. (a) Three-stage resistive feedback amplifier (1.63 mm×1.65 mm). (b) Wide-band gain response of three-stage resistive feedback amplifier.

V. DIGITAL IC CHIPS

The digital phase/frequency discriminator [7] and the digital prescaler were previous Hughes designs that were modified to meet the requirements of our PLL. FET channel characteristics were modified for processing compatibility with the analog circuits on the wafer, and digital circuit topology was customized for use in the PLL. All digital circuits use standard BFL with high- and low-impedance outputs to drive various load conditions.

Circuit performances of the two devices were well within the needs of the PLL. The phase/frequency discriminator operated up to 480 MHz. In the PLL, the A and the B output were resistively summed to allow full 180° phase detection. The prescaler chip operated up to 2.8 GHz, an improvement well over the 2.4 GHz result achieved with a previous iteration. At the 2.0 GHz PLL operating frequency, the prescaler produces a 125 MHz output signal at a power level of -3 dBm with no harmonically related spurs within the band of interest.

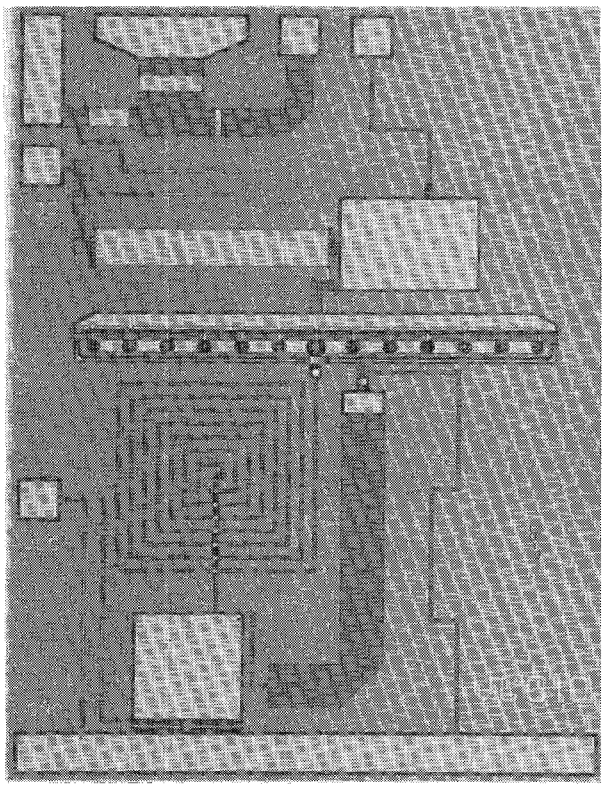


Fig. 4. Common-gate VCO (1.22 mm×1.55 mm).

VI. Voltage-Controlled Oscillator Chip

The VCO was initially realized as a MIC using bond wire inductance in series with the gate and the source of a 728 μm FET to obtain negative resistance over the band of interest. The common-gate FET configuration uses gate bias to control the frequency of oscillation. After successful operation of this circuit, the MMIC was designed with the same topology using spiral inductors (Fig. 4). However, the original MIC VCO was utilized for all test results presented in this report. The VCO's band of operation is 1.9 to 2.2 GHz, with an output power of +5 dBm.

VII. Phase-Locked Loop Integration

The PLL required the integration of nine circuit building blocks, each individually tested. Since ease of chip interchangeability of all circuits was desired, the monolithic chips were assembled onto individual 25 mil alumina substrates. The monolithic chips, the VCO, and a thin-film TaN 3 dB power splitter were integrated into the PLL housing. A first-order *RC* loop filter was inserted between the phase/frequency discriminator and VCO to control the overall loop response.

The locked loop, using an input reference frequency of 125 MHz, provided the 2 GHz spectrum plot shown in Fig. 5. Over the wide-band spectrum, no spurs were present. Under these operating conditions, preliminary phase noise performance of better than −70 dBc/Hz at a 10 kHz offset was measured at an output power level of −6 dBm. Total dc power consumption was 3 W. Lock range was limited to 350 kHz.

The PLL has the potential for improved performance by the incorporation of an active loop filter in place of the passive *RC* loop filter to increase the overall loop gain. The loop filter is the critical building block that determines the dynamic performance of the PLL. This includes the capture and lock ranges, bandwidth, and transient response. Because $1/f$ noise inherent in GaAs is a problem, the loop filter dc amplifier may have to be implemented in silicon and located off-chip in the final design. Adjustment of the active loop filter compensator will allow control of the PLL tracking and phase noise performance.

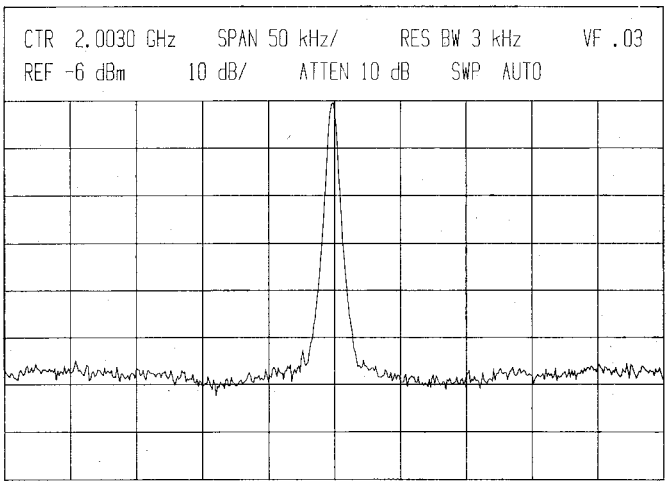


Fig. 5. Phase-locked loop performance.

VIII. Conclusion

Analog and digital MMIC chips for a 2.0 GHz phase-locked loop have been developed for space applications. MBE processing techniques that were implemented allow excellent analog and digital MMIC compatibility. The MMIC chips were used successfully in a 2.0 GHz single-breadboard phase-locked loop with a noise level of less than −70 dBc/Hz at a 10 kHz offset in a surface area of only 8 cm^2. The results attained by this research and development project should lead to further refinement of the PLL or development of a single-chip PLL.

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